Self Timed Power Efficient Full Adder

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ABSTRACT

In this paper we proposed a new design of single bit full adder cell. This design is based on adiabatic logic which is highly beneficial to reduce the energy consumption. To operate on low voltage levels we used dual pass transistor configuration which provides complementary energy path and hence supports adiabatic logic. Simulative investigation is done using Tanner EDA tool in 180nm technology. Results show very good performance of dual pass transistor configuration with complementary energy path (Adiabatic logic) at reduced energy consumption and on moderate speed.

Keywords— Adiabatic logic, Dual pass transistors, power delay product, full adder, power clock source.

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I. INTRODUCTION

Recently, the requirement for low power CMOS design has been steadily increasing. More and more research work is concentrated on low power solutions. Moore's law states that component density and performance of VLSI circuits doubles every year. Energy consumption and performance are the key criteria considered while designing VLSI circuits. The key components of digital computing are multipliers and arithmetic logic unit (ALU). Full adder is basic unit which determines functionality of ALU and multiplier. Micron technology is very advanced now days, which solved the issue of area requirements of computational design. Dimensions of the MOSFETs can be shrunk into sub-micron region as reported in [1].

Adiabatic logic is very good alternative to conventions CMOS designs to realize the low power design. Adiabatic logic configurations minimize the energy consumption to a great extent. The charges stored in circuit capacitors are recycled efficiently. Thus it avoids the energy dissipation as heat. Conventional designs use constant DC source to charge the capacitances whereas adiabatic logic families use time varying voltage supply as power source.

The following mathematical formula shows the lower limit on dynamic power consumption by CMOS design.

$$P_{diss} = 2\left(\frac{R.C_L}{T}\right)C_L.V_{DD}^2 + V_T^2.C_L \quad (1)$$

It shows If we increase the clock time period T greater than time constant RCL we can reduce the power dissipation in switching transition. The extra power dissipation due to threshold voltage drop VT is termed as non adiabatic loss and it can be reduce by reducing the VT. Now days VT can be kept lower up to 0.3V[2]. Various adiabatic logic circuits [1]-[10] have been proposed up till now which use multiple phase power clocks which are not suitable for high speed design, also using multiple phase power clock results in prolonged delay in the output. In contrast to this, single phase power clock is more suitable to reduce the delay problem and to reduce the control techniques and more important it is capable of operating at high speed.

This paper describes the same single power clock technique to improve the performance. To reduce the energy consumption dual pass transistor configuration with adiabatic logic is used.

II. AIM AND OBJECTIVES

A. Aim

Our aim is to design a new full adder cell which will consume less power and energy while performing the required event in comparison with the present technologies.

B. Objectives

We have proposed a new full adder cell based on asynchronous clocking combined with adiabatic logic which is faster as well as efficient in reducing the energy consumption. We used pulsed power clock source. We have tested the proposed circuit with varying the input frequency and pulsed power clock frequency. The detailed reading table is shown in results and outcomes.

NAND-NOR are the universal gates and are used to design complex digital circuits. XOR-XNOR are useful in larger circuits design such as full adder and parity checker. Optimised design using DPL-CEPAL is proposed and it is proved as beneficial as far as performance of the larger circuits is concerned.

III. ADIABATIC LOGIC DESIGN

Adiabatic is a Greek term and it is related with Thermodynamics. In adiabatic system transition occurs without energy (in form of heat) lost or gains from the system. In our design we used adiabatic logic to reduce the energy consumption. This differs from CMOS switching which dissipates energy during switching. Considering this technology it is clear that energy is reproduced and reused to perform further calculations.

To reduce the dynamic power some approaches are to decrease the physical capacitances and to reduce the switching activity. These techniques are not suitable for today's power requirement. Most of the work is being done on adiabatic logic design which is very beneficial for low power applications.

Adiabatic logic reduces the switching activities and it reduces the energy consumption. The basic concept is to give stored energy back to power source. Thus it is a simple reversible logic.

Following are the design rules for the adiabatic circuit design.

1. Never turn on a transistor if there is voltage across it. (VDS>0).
2. Never turn on a transistor if there is current flowing through it(IDS≠0).
3. Never pass current through a diode.

These are the conditions regarding the input in all the phases of power clock. Energy is stored in the recovery phase.

A. Limitations of Adiabatic logic

1. Circuit has to be implemented with time varying power source which is complex procedure.
2. Operating speed can be slower and my require more area than conventional CMOS.

B. Asynchronous adiabatic logic

It is a unique combination of energy saving benefits of adiabatic logic and asynchronous circuits. Asynchronous circuits have built-in sensitivity to variations in power supply voltage. Another advantage of this, in idle state it will not utilize clock signals whereas in synchronous circuits clock signal is given continuously to the entire system and thus it consumes energy and convert it into the heat.

The main advantage of this circuit is lower power consumption and no transistor ever changes the state unless it's performing a useful computation.

IV. METHODOLOGY ADOPTED

Dual pass transistors logic is useful to improve the circuit performance at reduced voltage level. For low voltage, low power and for small power delay dual pass logic is beneficial.[5][7] Pass transistor structure makes it easy to pull the sizing of transistors to get the desired charging and discharging time. Thus the slope of output signal minimizes the power.

Dual pass transistor logic is modified version of complementary pass transistor logic. Full swing operation is possible in dual pass logic. Problems of noise margin and speed degradation due to the use of reduced supply voltages are avoided. This is achieved by adding PMOS transistor in parallel with NMOS transistor.

In CMOS design the important part is to design the power clock because the complete transistor logic shares the same power clock and hence the power clock switching circuit dissipates the most of the power. In synchronous clocking the single clock is shared by large number of logical gates in parallel and hence the switching loss of power clock is more in synchronous clocked circuits.

In asynchronous clocking the energy is locally stored in and stored energy is fed back to power clock source and used for subsequent gates. This technique will help to save the power consumption. This approach is helpful while implementing the adiabatic logic in real time.

DPL-CEPAL (Dual pass logic-complementary energy path adiabatic logic) is efficiently implemented. DPL-CEPAL logic is composed of two PMOS switches to provide the complementary path to the stored energy. Through these switches the stored energy will be fed back to the power clock source. Dual pass logic is situated between clocked power source and constant DC source. The current flowing through the dual pass transistors will depend on the potential difference between clocked power source and constant DC source.

Above explained techniques are discussed in more details in the following sections. Proposed full adder cell is combination of logic part consisting DPL and CEPAL part to provide complementary energy path to reduce the energy consumption.

V. PROPOSED FULL ADDER CELL

Our objective is to design and implement energy efficient full adder cell using DPL-CEPAL. In DPL-CEPAL tow power sources are used one at top which is pulsed power clock and one at bottom which is constant DC or sometimes ground. Two PMOS switches are used to provide the complementary energy path at the top.

In DPL-CEPAL, output logic level is always slightly lower than input logic levels due to the non-adiabatic losses. The main concept is to carry the input signal to the output according to the digital logic.

Generally Complementary power clock is used in complementary energy path adiabatic logic. We have used pulsed power VDD source along with constant DC source.

A. DPL-CEPAL OR-NOR Logic

Fig. 1 shows proposed DPL-CEPAL OR-NOR logic with the associated waveforms.

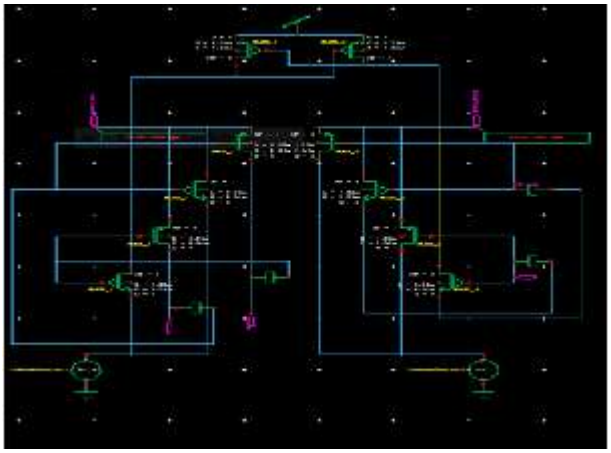

FIGURE 1. DPL-CEPAL OR-NOR LOGIC

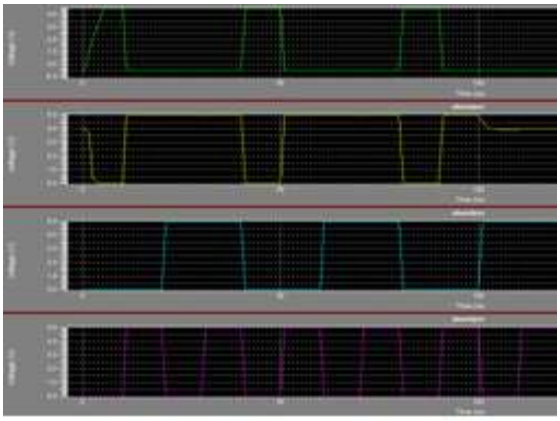

Figure 2. DPL-CEPAL OR-NOR waveforms

Fig. 2 shows the associated waveforms of DPL-CEPAL logic. VDD source is pulsed power clock and constant DC source is connected as shown. Two PMOS and two NMOS are connected as shown to form dual pass logic.

B. DPL-CEPAL AND-NAND Logic

Fig. 3 shows proposed DPL-CEPAL AND-NAND logic with the associated waveforms.

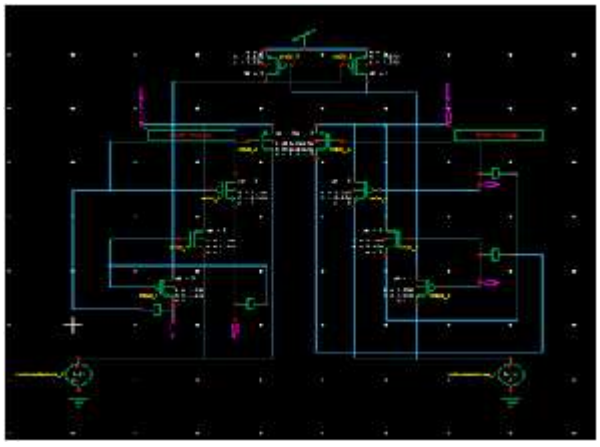

Figure 3. DPL-CEPAL AND-NAND Logic

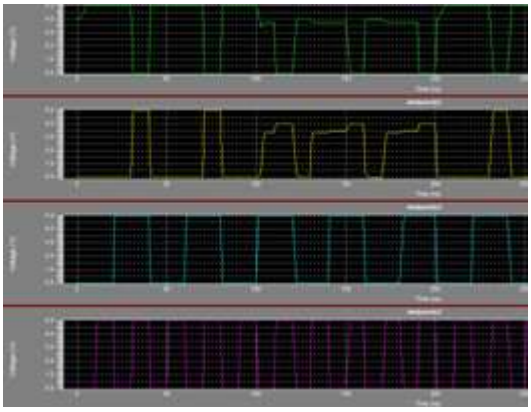

Figure 4. DPL-CEPAL AND-NAND waveforms.

Due to pulsed VDD source there is some propagation delay which will be measured to calculate the power delay product/energy.

C. DPL-CEPAL XOR-XNOR Logic

In the same way DPL-CEPAL XOR-XNOR logic is developed and shown with the associated waveforms in Fig. 5 and Fig. 6.

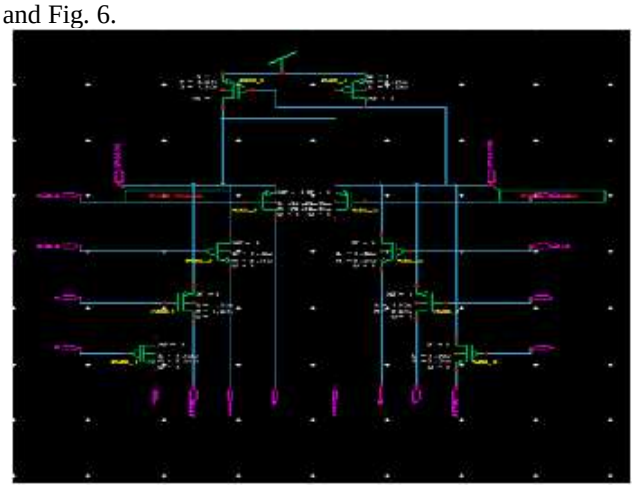

Figure 5. DEP-CEPAL XOR-XNOR Logic

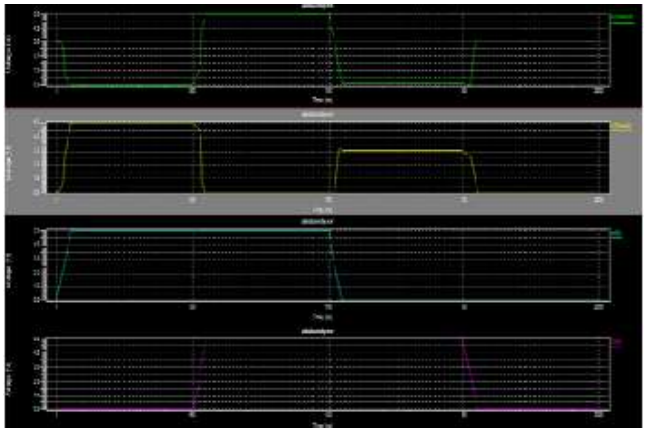

Figure 6. DPL-CEPAL XOR-XNOR waveforms.

D. Proposed DPL-CEPAL Full Adder cell

Using the above designed logics a simple full adder cell is designed as shown in Fig. 7 with associated waveforms.

All the schematics are done in Tanner EDA tool using 180 nm technologies. The pulsed VDD and DC source is 0.7V.

The results and outcomes section show the various reading taken to analyze the performance of the proposed design. As per the advancement in VLSI low power technology up to the year 2013 we can use 0.7V as VDD for MOS transistors with threshold voltage VT 0.3V. This helps reducing the power consumption. The lower nm technologies like 45nm can be used but if we go for lower dimensions technologies we have to use the higher VDD sources as lower dimension transistors can't pass the charges with the optimum speed and hence may cause longer propagation delays.

Thus it would become feasible to use the optimum voltage sources to reduce the propagation delay and noise margin.

From the obtained waveforms the propagation delay is measured and power delay product / energy can be calculated.

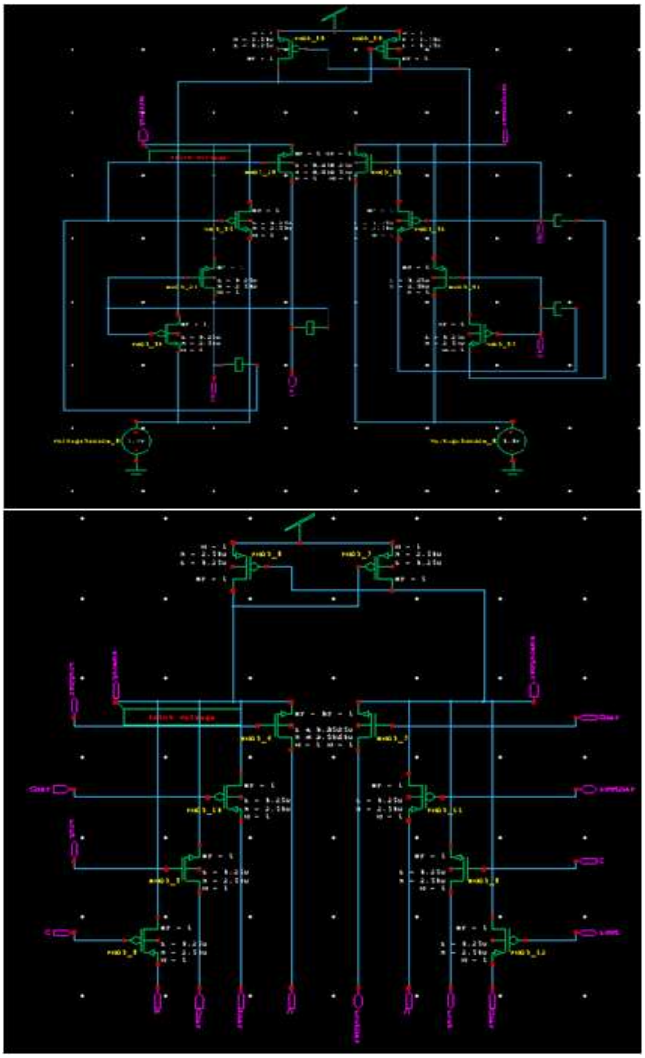

Figure 7. DPL-CEPAL Full Adder cell.

Functionality of 1 bit full adder cell with three input A, B and Cin(input carry) is described using equations:

$$Sum = A \oplus B \oplus Cin \quad (2)$$

$$C_{out} = A.B + Cin.(A+B) \quad (3)$$

Low power consumption is the target hence we used low power two input DPL-CEPAL XOR-XNOR logic for Sum circuit in our design. To generate, Cout is again implemented in the same way using DEL-CEPAL logic as shown in Fig. 7. The associated waveforms are shown in Fig. 8.

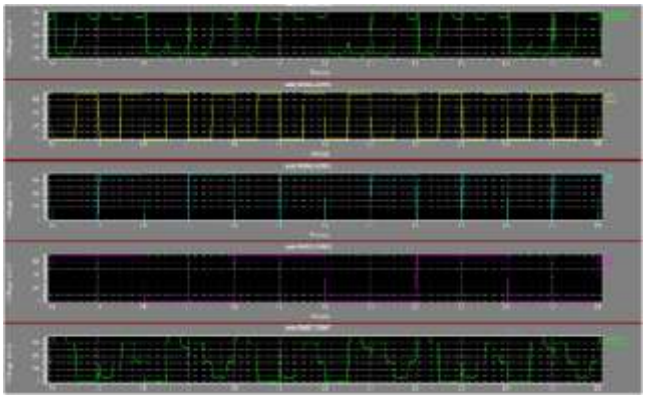

Figure 8. DPL-CEPAL Full Adder waveforms.

VI. Results and Outcomes

Our aim is to decrease to energy expended per switching operation. Only measuring the power consumption is not sufficient in CMOS design. A design can consume very low power to perform a particular operation at low frequency but may take very long time to finish the operation. Therefore it becomes necessary to measure the energy dissipation. Thus the performance of the CMOS design is analyzed by calculating the PDP(power delay product) which is product of average power consumption and propagation delay TD.[2][4]

The delay TD is measured from the instance of time the input reaches the 50% of its maximum value of power source to the instance that the instantaneous Sum and Cout signal reach the same voltage level.

PDP is calculated as[2]

$$PDP = Avg\ Power * T_D \quad (4)$$

The simulation results as shown in TABLE I give the readings of average power consumption.

TABLE I
AVERAGE POWER (VDD = 0.7V, VT = 0.3V) OF VARIOUS FULL ADDERS IN NANO-WATT.

V_{DD} POWER SOURCE	LOGIC DESIGNS	FREQUENCY IN MHZ			
		1	10	100	200
DC	CMOS	12.14	118	1830	3420
DC	TG	8.31	154.4	1560	3050
DC	PROPOSED DPL	115.7	1780	18860	33890
PULSE 50HZ	PROPOSED DPLCEPAL	3570	4800	17910	30230
PULSE 100KHZ	PROPOSED DPLCEPAL	3570	4800	17910	30230
PULSE 250KHZ	PROPOSED DPLCEPAL	2050	2440	9010	14980
PULSE 1MHZ	PROPOSED DPLCEPAL	1500	2130	9020	15010
PULSE 5MHZ	PROPOSED DPLCEPAL	1870	1090	8790	15550
PULSE 50MHZ	PROPOSED DPLCEPAL	2980	8790	8310	15530

PULSE 100MHZ	PROPOSED DPLCEPAL	2540	2970	7920	13540
PULSE 200MHZ	PROPOSED DPLCEPAL	1500	4790	17870	29990
PULSE WITH DOUBLE THE INPUT FREQUENCY	PROPOSED DPLCEPAL	1820	2610	4990	6230

Delay TD is recorded for Sum and Cout and as shown in following TABLEs II and III.

TABLE II
DEALY TD FOR SUM IN NANOSEC.

VDD POWER SOURCE	**LOGIC DESIGNS**	**FREQUENCY IN MHZ**			
		1	10	100	200
DC	CMOS	3	3	2.1	2.86
DC	TG	0.5	1	6	18
DC	PROPOSED DPL	0.4	2.9	2.9	0.8
PULSE 50HZ	PROPOSED DPLCEPAL	0.1	2.6	2.6	2.6
PULSE 100KHZ	PROPOSED DPLCEPAL	0.001	0.01	0.04	0.6
PULSE 250KHZ	PROPOSED DPLCEPAL	0.002	0.002	0.001	0.001
PULSE 1MHZ	PROPOSED DPLCEPAL	2.5	0.005	0.001	0.85
PULSE 5MHZ	PROPOSED DPLCEPAL	0.5	0.0005	0.6	0.6
PULSE 50MHZ	PROPOSED DPLCEPAL	0.0005	0.05	0.725	0.05
PULSE 100MHZ	PROPOSED DPLCEPAL	0.0005	0.325	0.325	0.325
PULSE 200MHZ	PROPOSED DPLCEPAL	0.0005	0.0005	0.0005	0.6
PULSE WITH DOUBLE THE INPUT FREQUENCY	PROPOSED DPLCEPAL	0.0005	0.0005	0.0005	0.3

The delay of proposed design is superior to the existing CMOS adiabatic logics. TABLE II and III shows same T_D for Sum and Cout.

TABLE III

DEALY TD FOR COUT IN NANOSEC.

VDD POWER SOURCE	LOGIC DESIGNS	FREQUENCY IN MHZ			
		1	10	100	200
DC	CMOS	3	3	2.1	2.86
DC	TG	0.5	1	6	18
DC	PROPOSED DPL	0.4	2.9	2.9	0.8
PULSE 50HZ	PROPOSED DPLCEPAL	0.1	2.6	2.6	2.6
PULSE 100KHZ	PROPOSED DPLCEPAL	0.001	0.01	0.04	0.6
PULSE 250KHZ	PROPOSED DPLCEPAL	0.002	0.002	0.001	0.001
PULSE 1MHZ	PROPOSED DPLCEPAL	2.5	0.005	0.001	0.85
PULSE 5MHZ	PROPOSED DPLCEPAL	0.5	0.0005	0.6	0.6
PULSE 50MHZ	PROPOSED DPLCEPAL	0.0005	0.05	0.725	0.05
PULSE 100MHZ	PROPOSED DPLCEPAL	0.0005	0.325	0.325	0.325
PULSE 200MHZ	PROPOSED DPLCEPAL	0.0005	0.0005	0.0005	0.6
PULSE WITH DOUBLE THE INPUT FREQUENCY	PROPOSED DPLCEPAL	0.0005	0.0005	0.0005	0.3

From these tables the PDP/energy is calculated using the equation (4).

TABLE IV shows PDP/Energy in Aj.

TABLE IV

PDP/ENERGY IN AJ

VDD POWER SOURCE	**LOGIC DESIGNS**	**FREQUENCY IN MHZ**			
		1	10	100	200
DC	CMOS	36.42	353.85	3843	9781.2
DC	TG	4.155	154.38	9360	54900
DC	PROPOSED DPL	46.272	5162	54694	27112
PULSE 50HZ	PROPOSED DPLCEPAL	357	12480	46566	78598
PULSE 100KHZ	PROPOSED DPLCEPAL	3.57	48	716.4	18138
PULSE 250KHZ	PROPOSED DPLCEPAL	4.1	4.88	9.01	14.98
PULSE 1MHZ	PROPOSED DPLCEPAL	3750	10.65	9.02	12758.5
PULSE 5MHZ	PROPOSED DPLCEPAL	935	0.545	5274	9330
PULSE 50MHZ	PROPOSED DPLCEPAL	1.49	439.5	6024.75	776.5
PULSE 100MHZ	PROPOSED DPLCEPAL	1.27	965.25	2574	4400.5
PULSE 200MHZ	PROPOSED DPLCEPAL	0.75	2.395	8.935	17994

PULSE WITH DOUBLE THE INPUT FREQUENCY	PROPOSED DPLCEPAL	0.91	1.305	2.495	1869

From TABLE IV it is clear that the PDP/energy is the lowest for pulse power clock frequency 200MHZ and when the pulse power clock frequency is double the input frequency. This shows that energy consumption is lowest when frequency of power clock is double the input frequency which is superior to the old adiabatic concepts.

This is shown graphically in Chart I.

TABLE V shows the PDP/energy comparison of the proposed full adder design with the existing technologies.

TABLE V
ENERGY (IN FJ) CONSUMPTION COMPARISON WITH EXISTING LOGICS

LOGIC DESIGNS	**FREQUENCY IN MHZ**			
	1	10	100	200
2N2P	3	5	7	15
2N2N2P	3	3	9	20
IPGL	15	13	25	40
ADSL	13	25	45	76
CMOS	0.03642	0.35385	3.843	9.781
TG	0.00416	0.15438	9.36	54.9
DPL	0.04627	5.162	54.694	27.11
DPL-CEPAL WITH PULSE 200MHZ	0.00075	0.0024	0.00894	17.99
DPL-CEPAL WITH PULSE FREQUENCY DOUBLE THE INPUT FREQUENCY	0.00091	0.00131	0.0025	1.869

From TABLE V it is clear that proposed design shows lowest energy consuption of the listed conventional adiabatic technologies at pulse power source frequencies 200MHZ and double the input frequency.

CHART I
ENERGY/PDP CHART

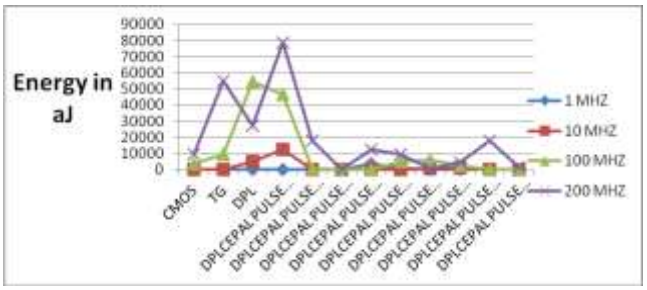

Chart II shows the PDP/energy comparision of the proposed full adder design with the existing technologies.

CHART II
ENERGY (IN FJ) CONSCUMPTION COMPARISION WITH EXISTING LOGICS

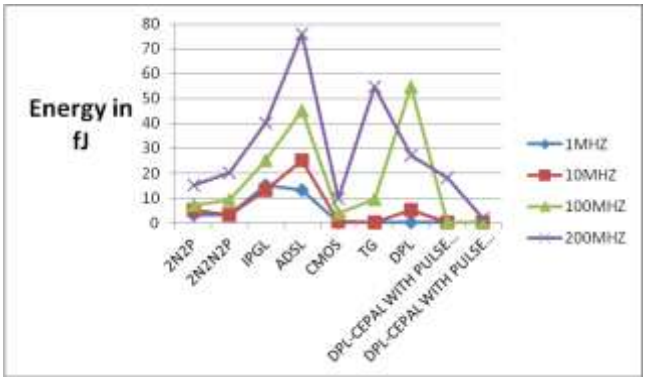

Chart II shows clearly that if frequency of pulsed power clock is maximum the energy consumption will be lowest.

In our readings, it shows best result if the frequency of pulsed power source is double the input frequency.

At last, the Transistor count comparision is shown in TABLE VI. As per the Moore's law the transistor count per squre inch doubles every year and it is quite evident in our design.

Though the number of transistors are increased in our proposed design we have succeeded in reducing the energy consumption efficiently.

TABLE VI
TRANSISTOR COUNT COMPARISION

LOGIC STYLE	**NO. OF TRANSISTORS**
CONVENTIONAL CMOS	28
TRANSMISSION GATES	20
DPL	48
DPTAAL	65
PROPOSED DPL	104
PROPOSED DPL-CEPAL	110

VII. CONCLUSIONS AND FUTURE SCOPE

From chart I and we can conclude that energy consumption is lowest for input frequencies 1MHZ, 10MHZ, 100MHZ and 200MHZ when DPL-CEPAL with pulse power clock is 200MHZ and when it is double the input frequency.

In chart II and TABLE V energy/PDP of proposed DPL-CEPAL is compared with the energy consumption of existing technologies. It clearly shows that proposed DPL-CEPAL performs very well when pulse power source frequency is 200MHZ and when it is double the input frequency.

A. Future scope

The proposed design can be tested for low on chip power density further. Though we have utilized the pulsed power source efficiently, propagation delay can further be reduced by more efficiently utilizing the pulsed power supply as VDD source. Further the performance of proposed schematic may be increased by checking noise margin and current at different nodes.

IC layout can be created by importing spice net list of the proposed schematic and LVS comparison is possible to compare the schematic design and IC layout.

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